CLAIMS:

1. An addressing mechanism, comprising:

a first set of parallel, co-planar conductive control lines;

a second set of parallel, co-planar conductive control lines, wherein said second set of conductive control lines are spaced apart in relation to said first set of conductive control lines, wherein a plane of said second set of conductive control lines is parallel to a plane of said first set of conductive control lines, wherein control lines of said second set of conductive control lines are perpendicular to control lines of said first set of conductive control lines;

a first select mechanism configured to selectively apply an in-line impedance to a control line of said first set of conductive control lines; and

a second select mechanism configured to selectively apply a drive voltage to each conductive line of said second set of conductive lines.

2. The addressing mechanism as recited in claim 1, wherein said first select mechanism is further configured to selectively toggle control lines of said first set of conductive control lines between a low impedance state and a high impedance state.

3. The addressing mechanism as recited in claim 2, wherein said first selected mechanism further comprises:

a row select sequencer configured to sequentially activate subsequent control lines in said first set of conductive control lines, wherein a selected control line in said first set of conductive control lines is placed in a low impedance state while non-selected control lines in said first set of conductive control lines are placed in a high impedance state;

a clock mechanism configured to determine a duration of time said selected control line is in said low impedance state; and

a synchronizing mechanism configured to synchronize loading and encoding of data to said clocking mechanism and said selected control line such that said data is loaded and processed during said duration of time said selected control line is in said low impedance state.

4. The addressing mechanism as recited in claim 1, wherein a region of overlap between a conductive line of said first set of conductive control lines and a conductive line of said second set of conductive control lines is selectively charged and discharged.

5. The addressing mechanism as recited in claim 4, wherein a cycle time for selectively charging and discharging said region of overlap is sufficiently short such that an active device will not be deactivated and an inactive device will not be activated, wherein said cycle time for selectively charging and discharging said region of overlap is sufficiently long such that an active device will discharge to below an activation threshold and an inactive device will charge beyond said activation threshold.

6. The addressing mechanism as recited in claim 1, wherein control lines in said second set of conductive control lines are equally split into two collinear, coplanar halves with sufficient physical separation to ensure electrical isolation between them.

7. The addressing mechanism sad recited in claim 1, wherein a polarity of a field generated between control lines of said first set of conductive control lines and control lines of said second set of conductive controls lines are reversed in a cyclic manner.

8. The addressing mechanism as recited in claim 7, wherein said polarity of said field is reversed in said cyclic manner by driving a pair of comparators from a voltage divider and oscillating a control logic signal distributed across appropriate reference potentials of opposing polarity.

9. The addressing mechanism as recited in claim 1, wherein said first set of parallel, co-planar conductive control lines and said second set of parallel, co-planar conductive control lines are driven at both ends from a common signal source.

10. The addressing mechanism as recited in claim 9, wherein a first set of voltage levels are applied to said first set of parallel, co-planar conductive control lines, wherein a second set of voltage levels are applied to said second set of parallel, co-planar conductive control lines, wherein an activated device at a region of overlap between a conductive line of said first set of conductive control lines and a conductive line of said second set of conductive control lines is deactivated when a difference between one of said second set of voltage levels and one of said first set of voltage levels is below a first threshold, wherein an activated device at said region of overlap is deactivated when a difference between one of said second set of voltage levels and one of said first set of voltage levels is less than a first threshold, wherein a deactivated device at said region of overlap is activated when a difference between one of said second set of voltage levels and one of said first set of voltage levels exceeds a second threshold.

11. The addressing mechanism as recited in claim 1, wherein each conductive line of said first set of parallel, co-planar conductive control lines comprises a material configured to selectively change its resistance across the entire conductive line.

12. The addressing mechanism as recited in claim 11, wherein said material of said first set of parallel, co-planar conductive control lines changes its resistance upon application of an appropriate potential difference between a first and a second conductive line spatially disposed on opposite sides of each conductive line of said first set of parallel, co-planar conductive control lines.

13. The addressing mechanism as recited in claim 12, wherein said material comprises doped perovskites.

14. A display, comprising:

a first set of parallel, co-planar conductive control lines;

a second set of parallel, co-planar conductive control lines, wherein said second set of conductive control lines are spaced apart in relation to said first set of conductive control lines, wherein a plane of said

second set of conductive control lines is parallel to a plane of said first set of conductive control lines, wherein control lines of said second set of conductive control lines are perpendicular to control lines of said first set of conductive control lines;

a matrix of pixels overlapping between said first set of parallel, co-planar conductive control lines and said second set of parallel, co-planar conductive control lines;

a first select mechanism coupled to said matrix of pixels, wherein said first select mechanism is configured to selectively apply an in-line impedance to a control line of said first set of conductive control lines; and

a second select mechanism coupled to said matrix of pixels, wherein said second select mechanism is configured to selectively apply a drive voltage to each conductive line of said second set of conductive lines.

15. The display as recited in claim 14, wherein said first select mechanism is further configured to selectively toggle control lines of said first set of conductive control lines between a low impedance state and a high impedance state.

16. The display as recited in claim 15, wherein said first selected mechanism further comprises:

a row select sequencer configured to sequentially activate subsequent control lines in said first set of conductive control lines, wherein a selected control line in said first set of conductive control lines is placed in a low impedance state while non-selected control lines in said first set of conductive control lines are placed in a high impedance state;

a clock mechanism configured to determine a duration of time said selected control line is in said low impedance state; and

a synchronizing mechanism configured to synchronize loading and encoding of data to said clocking mechanism and said selected control line such that said data is loaded and processed during said duration of time said selected control line is in said low impedance state.

17. The display as recited in claim 14, wherein a pixel of said matrix of pixels between a conductive line of said first set of conductive control lines and a conductive line of said second set of conductive control lines is selectively charged and discharged.

18. The display as recited in claim 17, wherein a cycle time for selectively charging and discharging said pixel of said matrix of pixels is sufficiently short such that an active device will not be deactivated and an inactive device will not be activated, wherein said cycle time for selectively charging and discharging said pixel of said matrix of pixels is sufficiently long such that an active device will discharge to below an activation threshold and an inactive device will charge beyond said activation threshold.

19. The display as recited in claim 14, wherein control lines in said second set of conductive control lines are equally split into two collinear, coplanar halves with sufficient physical separation to ensure electrical isolation between them.

20. The display as recited in claim 14, wherein a polarity of a field generated between control lines of said first set of conductive control lines and control lines of said second set of conductive controls lines are reversed in a cyclic manner.

21. The display as recited in claim 20, wherein said polarity of said field is reversed in said cyclic manner by driving a pair of comparators from a voltage divider and oscillating a control logic signal distributed across appropriate reference potentials of opposing polarity.

22. The display as recited in claim 14, wherein said first set of parallel, co-planar conductive control lines and said second set of parallel, co-planar conductive control lines are driven at both ends from a common signal source.

23. The display as recited in claim 22, wherein a first set of voltage levels are applied to said first set of parallel, co-planar conductive control lines, wherein a second set of voltage levels are applied to said second set of parallel, co-planar conductive control lines, wherein an activated device at a pixel of said matrix of pixels between a conductive line of said first set of conductive control lines and a conductive line of said second set of conductive control lines is deactivated when a difference between one of said second set of voltage levels and one of said first set of voltage levels is below a first threshold, wherein an activated device at said pixel of said matrix of pixels is deactivated when a difference between one of said second set of voltage levels and one of said first set of voltage levels is less than a first threshold, wherein a deactivated device at said pixel of said matrix of pixels is activated when a difference between one of said second set of voltage levels and one of said first set of voltage levels exceeds a second threshold.

24. The display as recited in claim 14, wherein each conductive line of said first set of parallel, co-planar conductive control lines comprises a material configured to selectively change its resistance across the entire conductive line.

25. The display as recited in claim 24, wherein said material of said first set of parallel, co-planar conductive control lines changes its resistance upon application of an appropriate potential difference between a first and a second conductive line spatially disposed on opposite sides of each conductive line of said first set of parallel, co-planar conductive control lines.

26. The display as recited in claim 25, wherein said material comprises doped perovskites.

27. A system, comprising:

a processor;

a memory unit;

an input mechanism;

a display; and

a bus system for coupling the processor to the memory unit, input mechanism and display;

wherein said display comprises:

a first set of parallel, co-planar conductive control lines;

a second set of parallel, co-planar conductive control lines, wherein said second set of conductive control lines are spaced apart in relation to said first set of conductive control lines, wherein a plane of said second set of conductive control lines is parallel to a plane of said first set of conductive control lines, wherein control lines of said second set of conductive control lines are perpendicular to control lines of said first set of conductive control lines;

a matrix of pixels overlapping between said first set of parallel, co-planar conductive control lines and said second set of parallel, co-planar conductive control lines;

a first select mechanism coupled to said matrix of pixels, wherein said first select mechanism is configured to selectively apply an in-line impedance to a control line of said first set of conductive control lines; and

a second select mechanism coupled to said matrix of pixels, wherein said second select mechanism is configured to selectively apply a drive voltage to each conductive line of said second set of conductive lines.

28. The system as recited in claim 27, wherein said first select mechanism is further configured to selectively toggle control lines of said first set of conductive control lines between a low impedance state and a high impedance state.

29. The system as recited in claim 28, wherein said first selected mechanism further comprises:

a row select sequencer configured to sequentially activate subsequent control lines in said first set of conductive control lines, wherein a selected control line in said first set of conductive control lines is placed in a low impedance state while non-selected control lines in said first set of conductive control lines are placed in a high impedance state;

a clock mechanism configured to determine a duration of time said selected control line is in said low impedance state; and

a synchronizing mechanism configured to synchronize loading and encoding of data to said clocking mechanism and said selected control line such that said data is loaded and processed during said duration of time said selected control line is in said low impedance state.

30. The system as recited in claim 27, wherein a pixel of said matrix of pixels between a conductive line of said first set of conductive control lines and a conductive line of said second set of conductive control lines is selectively charged and discharged.

31. The system as recited in claim 30, wherein a cycle time for selectively charging and discharging said pixel of said matrix of pixels is sufficiently short such that an active device will not be deactivated and an inactive device will not be activated, wherein said cycle time for selectively charging and discharging said pixel of said matrix of pixels is sufficiently long such that an active device will discharge to below an activation threshold and an inactive device will charge beyond said activation threshold.

32. The system as recited in claim 27, wherein control lines in said second set of conductive control lines are equally split into two collinear, coplanar halves with sufficient physical separation to ensure electrical isolation between them.

33. The system as recited in claim 27, wherein a polarity of a field generated between control lines of said first set of conductive control lines and control lines of said second set of conductive controls lines are reversed in a cyclic manner.

34. The system as recited in claim 33, wherein said polarity of said field is reversed in said cyclic manner by driving a pair of comparators from a voltage divider and oscillating a control logic signal distributed across appropriate reference potentials of opposing polarity.

35. The system as recited in claim 27, wherein said first set of parallel, co-planar conductive control lines and said second set of parallel, co-planar conductive control lines are driven at both ends from a common signal source.

36. The system as recited in claim 35, wherein a first set of voltage levels are applied to said first set of parallel, co-planar conductive control lines, wherein a second set of voltage levels are applied to said second set of parallel, co-planar conductive control lines, wherein an activated device at a pixel of said matrix of pixels between a conductive line of said first set of conductive control lines and a conductive line of said second set of conductive control lines is deactivated when a difference between one of said second set of voltage levels and one of said first set of voltage levels is below a first threshold, wherein an activated device at said pixel of said matrix of pixels is deactivated when a difference between one of said second set of voltage levels and one of said first set of voltage levels is less than a first threshold, wherein a deactivated device at said pixel of said matrix of pixels is activated when a difference between one of said second set of voltage levels and one of said first set of voltage levels exceeds a second threshold.

37. The system as recited in claim 27, wherein each conductive line of said first set of parallel, co-planar conductive control lines comprises a material configured to selectively change its resistance across the entire conductive line.

38. The system as recited in claim 37, wherein said material of said first set of parallel, co-planar conductive control lines changes its resistance upon application of an appropriate potential difference between a first and a second conductive line spatially disposed on opposite sides of each conductive line of said first set of parallel, co-planar conductive control lines.

39. The system as recited in claim 38, wherein said material comprises doped perovskites.